INICORE
System-on-Chip from Spec to Silicon

Optimized for Actel

# VME64 Slave Controller

## Description

The VMEbus was first standardized in 1981 and is still in wide use. With the advances in integration technologies, custom integrated VME controllers open the door for smaller and cheaper systems. Inicore offers a wide range of different VME slave controllers. Each one optimized for a certain application. The difference lies mainly in the address and data bus width and the supported data modes.

The VME slave controller shields all the complexity of the asynchronous VMEbus and provides an easy-to-use, synchronous parallel user side interface towards custom logic. A built-in interrupter handles all local interrupt requests and acknowledgments.

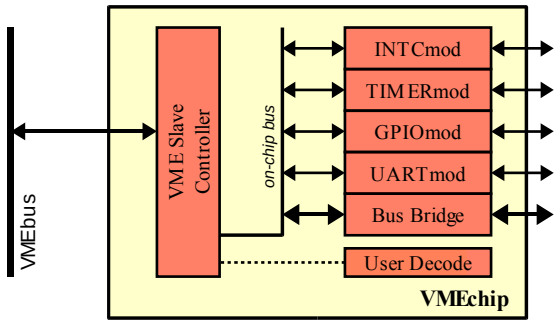


*Figure 1: Sample application*

The figure above illustrates a typical application where several peripheral functions together with the VME slave core as well as a bus bridge are integrated into one FPGA.

### Supported modes

- Data modes: D8, D16, D32
- Address modes: A16, A24, A32
- Access modes: Read, write, read-modify-write, D32-BLT, MBLT
- Interrupter: D8, D16, D32, RORA, ROAK

## Features

- ANSI/VITA 1-1994 compliant
- VME slave controller
- Data modes: D8, D16, D32
- Address modes: A16, A24, D32
- Supports read, write, read-modify-write, D32-BLT and MBLT cycles
- Configurable D8, D16 or D32 interrupter
- Fully synchronous user side interface
- User selectable wait-states
- Synchronous design

## Applications

- Industrial control
- Military
- Aerospace
- Telecom
- Medical

## Sample Utilization and Performance Table Optimized for Actel Devices

| Family | Device | Utilization | | | | | Performance |
|---|---|---|---|---|---|---|---|
| | - (speed grade) | s-mod | c-mod | Tiles | RAM | Total | [MHz] |
| ProASIC PLUS | APA600 | | | 729 | | 3% | 43 |
| Axcelerator | AX500-3 | 225 | 354 | | | 7% | 101 |
| SXA | SX72A-3 | 225 | 355 | | | 10% | 74 |
| RTSX | RTSX72S-1 MIL | 223 | 334 | | | 10% | 47 |

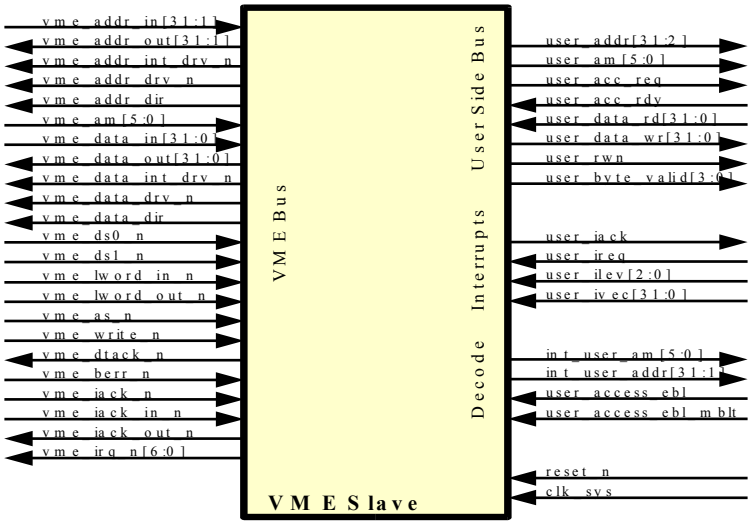


*Figure 2: Symbol*

## Interfaces

| Pin Name | Type | Description |
|---|---|---|
| **Global Signals** | | |
| clk | in | System clock |
| reset_n | in | Asynchronous system reset, active low |
| **VME Bus** | | |
| vme_addr_in[31:1] | in | Address bus input |
| vme_addr_out[31:1] | out | Address bus output |
| vme_addr_int_drv_n | out | Internal i/o driver enable |
| vme_addr_drv_n | out | External address bus driver enable |
| vme_addr_dir | out | External address bus driver direction |
| vme_am[5:0] | in | Address modifier code |
| vme_data_in[31:0] | in | Data bus input |
| vme_data_out [31:0] | out | Data bus output |
| vme_data_int_drv_n | out | Internal i/o driver enable |
| vme_data_drv_n | out | External data bus driver enable |
| vme_data_dir | out | External data bus driver direction |
| vme_ds0_n | in | Data strobe 0 |
| vme_ds1_n | in | Data strobe 1 |
| vme_lword_in_n | in | Long word indicator, in |
| vme_lword_out_n | out | Long word indicator, out |
| vme_as_n | in | Address strobe |
| vme_write_n | in | Read write not indicator |
| vme_dtack_n | out | Data acknowledge |
| vme_berr_n | in | Bus error |
| vme_iack_n | in | Interrupt acknowledge |

| Pin Name | Type | Description |
|---|---|---|
| vme_iack_in_n | in | Interrupt acknowledge chain in |
| vme_iack_out_n | out | Interrupt acknowledge chain out |
| vme_irq_n[6:0] | out | Interrupt request |
| **User Side Bus** | | |
| user_addr[31:2] | out | Address bus |
| user_am[5:0] | out | Address modifier code |
| user_acc_req | out | Data access request |
| user_acc_rdy | in | Data access request ready |
| user_data_rd[31:0] | in | Data read bus |
| user_data_wr[31:0] | out | Data write bus |
| user_rwn | out | Data read or write access |
| user_byte_valid [3:0] | out | Data byte valid |
| **User Decode** | | |
| int_user_addr[31:1] | out | Address bus |
| int_user_am[5:0] | out | Address modifier code |
| user_access_ebl | in | Valid user access |
| user_access_ebl_ mblt | in | Valid user access mblt mode |
| **Interrupt** | | |
| user_iack | out | Interrupt acknowledge |
| user_ireq | in | Interrupt request |
| user_ivec[31:0] | in | Interrupt vector |
| user_ilevel[2:0] | in | Interrupt request level |

## About Inicore

- FPGA and ASIC Design
- Easy-to-use IP Cores
- System-on-Chip Solutions
- Consulting Services
- ASIC to FPGA Migration
- Obsolete ASIC Replacements

Inicore is an experienced system design house providing FPGA / ASIC and SoC design services. The company's expertise in architecture, intellectual property, methodology and tool handling provides a complete design environment that helps customers shorten their design cycle and speed time to market. Our offering covers feasibility study, concept analysis, architecture definition, code generation and implementation. When ready, we deliver you a FPGA or take your design to an ASIC provider, whatever is more suitable for your unique solution.

## Deliverables

The core is available as Actel optimized netlist or as RTL version.

Actel Optimized Netlist:

- Netlist for target FPGA, EDIF, Verilog and VHDL format
- User Guide

RTL Source Code:

- VHDL or Verilog source code
- Funtional verification testbench
- Synthesis script
- Timing constraints
- User guide



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